UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,122	09/19/2001	Rami Rahim	0023-0041	8433

44987 7590 06/28/2005

HARRITY & SNYDER, LLP
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

EXAMINER	
PARK, JUNG H	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,122	RAHIM ET AL.	
	Examiner	Art Unit	
	Jung Park	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 5,6,11,14,15,26,27,30 and 31 is/are allowed.

6)☒ Claim(s) 1-4,7-10,12,13,16-25,28 and 29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending for the examination.

Specification

2. The disclosure is objected to because of the following informalities: There is a minor error in the specification. The "packet order table ("POC") (pp. 10, para. 37) should be changed to -- packet order table ("POT") --.

Appropriate correction is required.

Claim Objections

3. Claims 1 and 18 are objected to because of the following informalities: The meaning of "pipeline stages that together simultaneously operate" is not clear since the pipeline stages sequentially includes 10 stages (601-610 figure 6; pp. 13, para. 43) and each stage can be applied on the data items sequentially. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 7, 8, 12, 13, 18-20, 28, and 29 are rejected under 35 U.S.C 102(e) as being anticipated by Laor et al. (U.S. 6,831,923, "Laor").

Regarding claims 1 and 18, Laor teaches a reorder engine for reordering (222 figure 2A, col. 5, lines 10-15), on a per-entity basis (221 figure 2A), out-of-order data items, the reorder engine comprising:

a pipeline including a plurality of pipeline stages (210, 220, and 230, figure 2A) that together simultaneously operate on the data items (*packet header*, figure 1; col. 3, lines 17-20); and

per-entity context memories (223, figure 2A) operatively coupled to the pipeline stages, the per-entity context memories storing information relating to a state of reordering for each of the entities (223, figure 2A, col. 4, lines 44-46 and 57-64), the pipeline stages reading from and updating the context memories (*pipeline flow control and data flow among 221, 222, and 232,* figure 2A) based on the entity of the data item being processed.

Regarding claims 12 and 28, Laor teaches a method of reordering data items comprising:

receiving the data items associated with a plurality of entities (between 221 and 222, figure 2A);

inputting the received data items into a pipelined reorder engine (222 figure 2A); and

sequentially forwarding each of the input data items through stages of the pipelined reorder engine that reorders the received data items on a per-entity basis to corresponding to a transmitting order of the data items (222 and 230, figure 2A).

Regarding claim 7, the reorder buffer storing information relating to the received data items (223 figure 2A).

Regarding claim 8, Laor the reorder buffer is implemented as a circular memory (412 figure 4).

Regarding claims 13 and 29, the stages of the pipeline perform functions including:

determining which of the received data items to process based on an entity that transmitted the data item (between 221 and 222, figure 2A).

Regarding claims 19 and 20, they are claims corresponding to claim 1 and are therefore rejected for the similar reasons set forth in the rejection of claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laor.

Regarding claims 9 and 21, Laor is silent on the context memories including a pointer to each of the reorder buffers that references the real-most entry in the reorder buffer. The selection of a pointer to a position of memory is one to design choice with data processing system. Hence, it would have been obvious to combine this design choice with Laor for the purpose of locating the pointer to real-most position in the memory. The motivation is to indicate the pointer to the real-most position in the memory in order to utilize the memory well according to design method.

8. Claims 2, 3, 16, 17, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laor in view of admitted prior art (Admission).

Regarding claims 2, 16 and 23, Laor does not disclose expressly the entities connected to the reorder engine via a switch fabric and the network devise which is a router. However, admission teaches that a switching fabric or other transmission medium may be implemented in the router to carry the packets between the ports (pg. 2, para. 4). Therefore, it would have been obvious that the Laor's reorder engine is connected to the system via switch fabric and the network device is a router. The motivation is to employ a different type of transmission medium including the switch fabric and routers as the network device in order to convey many different type of traffic in the communication networks.

Regarding claims 3, 17 and 24, Laor does not disclose expressly that the data items are cells and wherein a plurality of cells comprise a packet. However, admission

teaches that the information is transmitted in discrete quantities called packets, or broken down even further into a series of cells (pg. 2, para. 4). Therefore, it would have been obvious to have cells or packets as the type of data items in Laor's system because one would be motivated to use different type of packet sizes to be used for different protocols.

9. Claims 4 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laor in view of Dell et al., U.S. Pub. No. (2002/0085578, "Dell") and Saito et al. U.S. Patent (4,907,147, "Saito").

Regarding claims 4 and 25, Laor fails to teach about the pipeline stages including at least one arbitrary stage that determines an active entity to process: However, Dell teaches that a bid arbitrator implemented as part of the switching stage determines whether to accept or reject the bid received for the input stage (col. 1 para. 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to combine the feature in Dell with Laor for the purpose of including at least one arbitration stage in the pipeline stages because one would be motivated to check an active entity for the purpose of processing.

Laor is silent on the address computation stage that is widely used in data processing system. However, Saito teaches that the address computation (32 figure 4) is one of the pipeline stages for the purpose of data processing. Therefore, it would have been obvious to have used the address computation stage in the system of Laor as taught by Saito because one would be motivated to include this stage as one of the pipeline processing stages in order to process data items.

10. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laor in view of Paatela et al., U.S. Pub. No. (2002/0163935, "Paatela").

Regarding claims 10 and 22, Laor fails to teach the context memories including a valid bit array associated with each of the reorder buffers, the valid bit array indicating whether entries in the reorder buffer are valid. However, Paatela teaches about the valid bit array (750, figure 7; col. 8, para. 80) associated with a portion of the memory (716 figure 7; col. 8, para. 80) in order to indicate whether or not the corresponding memory portion is storing valid data. (col. 8, para. 80). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to combine the feature in Paatela with Laor in order to apply this valid bit pattern to know the validation of entries in the reorder buffer.

Allowable Subject Matter

11. Claims 5, 14, 15, 26, 30, and 31 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest the modulo operation of the sequence number to know the position of the received data item. It is noted that the closest prior art, Meyer et al. (U.S. Pub. No. 2003/0,191,844) show about modulo operation to determine the maximum value of sequence number generated by transmitter, but Meyer does not teach about how to know the position of the received data items calculated based on a modulo operation.

Claims 6, 11, and 27 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest one of the pipeline stages configured to an assembly memory with information identifying a correct order of the data items on a per-entity basis.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Pub. No. (2003/0,005,164) to Trainin shows that sequence number is used to calculate a buffer's offset address and the data size is used to determine whether there is enough space in the buffer for received data.
- U.S. Patent (6,757,284) to Galles shows that a pipeline of sorting stages is used to order the one or more sets of streams of data items.
- U.S. Patent (6,226,687) to Harriman shows that a first stage of data packet processing, which sequentially receives a plurality of independent data packets.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung Park whose telephone number is 571-272-8565. The examiner can normally be reached on Mon-Fri during 7:15-4:45.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jung Park
Patent Examiner
June 22, 2005

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600